

LISTING OF THE CLAIMS

The following is a complete listing of the pending claims with a status identifier in parentheses. As no amendments are being presented in this response, there is no underlined text indicating insertions or strikethrough and/or double-bracketed text indicating deletions in any of the listed claims.

LISTING OF CLAIMS

1. (ORIGINAL) A semiconductor package comprising:
 - a substrate having a top surface and a bottom surface, the top surface including a plurality of substrate pads;
 - a semiconductor chip mounted on the substrate, the semiconductor chip having an active surface, a back surface, and a peripheral surface, the active surface including a plurality of chip pads;
 - a peripheral sealing portion formed along the peripheral surface of the semiconductor chip; and
 - a plurality of pattern leads providing electrical connections between chip pads and substrate pads, the pattern leads extending along an inclined surface of the peripheral sealing portion.
2. (ORIGINAL) A semiconductor package according to claim 1, further comprising:
 - an encapsulant covering the semiconductor chip, the peripheral sealing portion, the substrate pads and the pattern leads.

3. (ORIGINAL) A semiconductor package according to claim 1,
wherein:

the peripheral sealing portion covers a peripheral portion of the
active surface.

4. (ORIGINAL) A semiconductor package according to claim 2, further
comprising:

external connection terminals formed on the substrate, the external
connection terminals being electrically connected to the substrate pads.

5. (ORIGINAL) A semiconductor package according to claim 4,
wherein:

the external connection terminals are arranged on the bottom surface
of the substrate and are selected from a group consisting of solder balls, solder
bumps, microsprings and connecting pins.

6. (ORIGINAL) A semiconductor package according to claim 4,
wherein:

the external connection terminals are arranged on the top surface of
the substrate.

7. (ORIGINAL) A semiconductor package according to claim 1,
wherein:

the inclined surface of the peripheral sealing portion forms an angle
of between about 30 and 75 degrees relative to the top surface of the substrate.

8. (ORIGINAL) A semiconductor package according to claim 1,
wherein:

the peripheral sealing portion includes an insulating composition selected from a group consisting of photo solder resists and plastic resins.

9. (ORIGINAL) A semiconductor package comprising:

a substrate having a top surface and a bottom surface, the top surface including a plurality of substrate pads;

a semiconductor chip mounted on the substrate, the semiconductor chip having an active surface, a back surface, and a peripheral surface, the active surface including a plurality of chip pads;

a first peripheral sealing portion formed along the peripheral surface of the semiconductor chip;

a plurality of first pattern leads providing electrical connections between a first group of chip pads and a first group of substrate pads, the first pattern leads extending along an inclined surface of the first peripheral sealing portion;

a second peripheral sealing portion formed along the first peripheral sealing portion and the first pattern leads; and

a plurality of second pattern leads providing electrical connections between a second group of chip pads and a second group of substrate pads, the second pattern leads extending along an inclined surface of the second peripheral sealing portion.

10. (ORIGINAL) A semiconductor package according to claim 9, wherein:

a second pattern lead extends across a first pattern lead, electrical connection between the second pattern lead and the first pattern lead being prevented by an interposed portion of the second peripheral sealing portion.

11. (ORIGINAL) A semiconductor package according to claim 9,
wherein:

the first group of chip pads is completely separate from the second
group of chip pads.

12. (ORIGINAL) A semiconductor package according to claim 9,
wherein:

at least one chip pad is included in both the first group of chip pads
and the second group of chip pads.

13. (ORIGINAL) A semiconductor package according to claim 9, further
comprising:

an encapsulant covering the semiconductor chip, the first peripheral sealing
portion, the substrate pads, the first pattern leads, the second peripheral sealing
portion and the second pattern leads.

14. (ORIGINAL) A semiconductor package according to claim 9,
wherein:

the first peripheral sealing portion covers a first peripheral portion of
the active surface; and

the second peripheral sealing portion covers a second peripheral
portion of the active surface.

15. (ORIGINAL) A semiconductor package according to claim 9, further
comprising:

external connection terminals formed on the substrate, the external
connection terminals being electrically connected to the substrate pads.

16. (ORIGINAL) A semiconductor package according to claim 15,
wherein:
the external connection terminals are arranged on the bottom surface
of the substrate and are selected from a group consisting of solder balls, solder
bumps, microsprings and connecting pins.

17. (ORIGINAL) A semiconductor package according to claim 15,
wherein:
the external connection terminals are arranged on the top surface of
the substrate.

18. (ORIGINAL) A semiconductor package according to claim 9,
wherein:
the inclined surface of the first peripheral sealing portion forms an
angle of between about 30 and 75 degrees relative to the top surface of the
substrate; and
the inclined surface of the second peripheral sealing portion forms
an angle of between about 30 and 75 degrees relative to the top surface of the
substrate.

19. (ORIGINAL) A semiconductor package according to claim 9,
wherein:
the first and second peripheral sealing portions include an insulating
composition selected from a group consisting of photo solder resists and plastic
resins.

20. (ORIGINAL) A method for manufacturing a semiconductor package comprising:

mounting a semiconductor chip on a substrate, the semiconductor chip having a plurality of chip pads on an active surface and the substrate having a plurality of substrate pads on a top surface;

forming a first peripheral sealing portion, the first peripheral sealing portion enclosing a peripheral surface of the semiconductor chip and having an inclined surface;

forming first pattern leads to establish electrical connections between a first group of the chip pads and a corresponding first group of the substrate pads, the first pattern leads being formed on the inclined surface of the first peripheral sealing portion.

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